ABSRACT OF THE DISCLOSURE

In a clock supply control apparatus and method of the invention, a clock signal is generated, and supply of the generated clock signal from a clock supply logic unit to a second device of a computer system is controlled in response to a clock control signal, the second device being operable with the clock signal supplied from the clock supply logic unit. The clock control signal is set at one of a supply inhibition level and a supply allowance level in response to a state of a clock run signal line, the resulting clock control signal being supplied to the clock supply logic unit. A first device of the computer system is operable with the generated clock signal and outputs an interrupt signal to an interrupt signal line regardless of whether the clock control signal is set at the clock supply inhibition level or the clock supply allowance level.